

ZERO OVERHEAD COMPUTER INTERRUPTS  
WITH TASK SWITCHING

ABSTRACT OF THE DISCLOSURE

5           The invention constitutes a unique hardware  
zero overhead interrupt and task change mechanism for the  
reduction or elimination of interrupt latency and task  
change processing overhead delays in computer  
architectures. Without loss of time, the system performs  
10 complete task state saving and restoration between one  
cycle and the next without software intervention. For  
each Central Processing Unit (1) register, the invention  
uses one or more auxiliary latches (3, 4) wherein one  
latch (3, 4) is used as the "running" latch and one of  
15 the auxiliary latches is attached to task storage memory.  
The invention swaps connections between alternate  
"running" registers and auxiliary registers while  
transferring other tasks to and from task storage memory  
(2). The invention provides a task linking system to  
20 allow the linking of tasks for the mandatory sequential  
execution of the linked tasks. Further, the invention  
includes a priority "impatience" counter system to  
increase the relative priorities of various tasks as they  
approach their task deadlines.

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